IN THE CLAIMS

1. (Original) A memory device comprising:

a plurality of banks, each including a plurality of memory cores;

a plurality of sense amplifiers shared among memory cores of different ones of the plurality of banks; and

wherein the memory cores from two of the different ones of the plurality of banks are interleaved in a strip with the plurality of shared sense amplifiers.

2. (Original) The memory device of claim 1 wherein the strip is arranged in a row, and column decode conductors traverse the memory cores in the strip.

3. (Original) The memory device of claim 2 further comprising sense nodes substantially parallel to the column decode conductors.

4. (Original) The memory device of claim 1 wherein the plurality of memory cores are arranged into a plurality of strips, each strip including interleaved memory cores from two different ones of the plurality of banks.

5. (Original) A memory device comprising:

a plurality of memory cores logically arranged into a plurality of banks;

a plurality of sense amplifiers shared among memory cores of two of the plurality of banks; and

wherein the memory cores of the two of the plurality of banks are interleaved in a row.

6. (Original) The memory device of claim 5 further comprising column decode conductors for the row, the column decode conductors for the row being coupled to the plurality of sense amplifiers shared among the memory cores of the two of the plurality of banks.

7. (Original) The memory device of claim 6 wherein the plurality of memory cores are arranged in a plurality of rows and a plurality of columns, each of the plurality of rows including interleaved memory cores from two different ones of the plurality of banks.

8. (Original) The memory device of claim 5 wherein the plurality of memory cores are arranged in a plurality of rows and a plurality of columns, each of the plurality of rows including interleaved memory cores from two different ones of the plurality of banks.

9. (Original) A memory device comprising:

a first bank of memory cores arranged in a strip;

a second bank of memory cores interleaved with the first bank of memory cores arranged in the strip; and

a plurality of sense amplifiers shared between memory cores of the first bank and memory cores of the second bank.

10. (Original) The memory device of claim 9 further comprising a plurality of rows and a plurality of columns, wherein the strip is one of the plurality of rows.

11. (Original) The memory device of claim 10 wherein each of the plurality of rows includes interleaved memory cores from two different banks.

12. (Original) The memory device of claim 9 wherein each of the plurality of sense amplifiers is coupled to one memory core of the first bank and one memory core of the second bank.

13. (Original) The memory device of claim 9 further comprising a plurality of rows and a plurality of columns, wherein the strip is one of the plurality of columns.

14. (Original) A memory device comprising:

a first bank of memory cores arranged in a strip;

a second bank of memory cores interleaved with the first bank of memory cores arranged in the strip;

a plurality of sense amplifiers shared between memory cores of the first bank and memory cores of the second bank; and

a column decoder arranged to drive column decode lines coupled to the plurality of sense amplifiers.

15. (Original) The memory device of claim 14 further comprising a plurality of rows and a plurality of columns, wherein the strip is one of the plurality of rows.

16. (Original) The memory device of claim 15 wherein each of the plurality of rows includes interleaved memory cores from two different banks.

17. (Original) The memory device of claim 14 wherein each of the plurality of sense amplifiers is coupled to one memory core of the first bank and one memory core of the second bank.

18. (Original) An integrated circuit comprising:

an array of memory cores having a first dimension and a second dimension; and

wherein a strip of memory cores in the first dimension includes memory cores from a first bank interleaved with memory cores from a second bank.

19. (Original) The integrated circuit of claim 18 wherein the first dimension includes a plurality of rows of memory cores, and the second dimension includes a plurality of columns of memory cores, and each of the plurality of rows includes interleaved memory cores from two different banks.

20. (Original) The integrated circuit of claim 19 wherein each of the plurality of columns includes non-interleaved memory cores from different banks.

21. (Original) The integrated circuit of claim 18 further comprising:

a column decoder; and

a plurality of column decode conductors driven by the column decoder and situated substantially parallel to the strip of memory cores.

22. (Original) An integrated circuit comprising:

an array of memory cores having a first dimension and a second dimension, wherein a strip of memory cores in the first dimension includes memory cores from a first bank interleaved with memory cores from a second bank; and

a plurality of sense amplifiers arranged between memory cores from the first bank and memory cores from the second bank.

23. (Original) The integrated circuit of claim 22 wherein:

the first dimension includes a plurality of rows of memory cores;

the second dimension includes a plurality of columns of memory cores; and

each of the plurality of rows includes interleaved memory cores from two different banks.

24. (Original) The integrated circuit of claim 23 wherein each of the plurality of columns includes non-interleaved memory cores from different banks.

25. (Original) The integrated circuit of claim 22 further comprising:

a column decoder; and

a plurality of column decode conductors driven by the column decoder, coupled to the plurality of sense amplifiers, and situated substantially parallel to the strip of memory cores.

26. (Original) An integrated circuit comprising:

an array of memory cores having a first dimension and a second dimension, wherein a strip of memory cores in the first dimension includes memory cores from a first bank interleaved with memory cores from a second bank;

a plurality of sense amplifiers arranged between memory cores from the first bank and memory cores from the second bank; and

column decode conductors coupled to the plurality of sense amplifiers, the column decode conductors arranged to be near memory cores of the first and second bank, and not near memory cores of other banks.

27. (Original) The integrated circuit of claim 26 wherein the first dimension includes a plurality of rows of memory cores, and the second dimension includes a plurality of columns of memory cores, and each of the plurality of rows includes interleaved memory cores from two different banks.

28. (Original) The integrated circuit of claim 27 wherein each of the plurality of columns includes non-interleaved memory cores from different banks.

29. (Original) A memory device comprising:

a first bank of memory cores;

a second bank of memory cores; and

a plurality of sense amplifiers shared between the first bank of memory cores and the second bank of memory cores;

wherein the first bank of memory cores and the second bank of memory cores are interleaved in a first row on the memory device.

30. (Original) The memory device of claim 29 further comprising:

a plurality of rows of which the first row is one; and

a plurality of columns of memory cores, each of the plurality of columns of memory cores having non-interleaved memory cores from a plurality of banks.

31. (Original) The memory device of claim 29 further comprising:

a third bank of memory cores;

a fourth bank of memory cores; and

a plurality of sense amplifiers shared between the third bank of memory cores and the fourth bank of memory cores;

wherein the third bank of memory cores and the fourth bank of memory cores are interleaved in a second row parallel to the first row.

32. (Original) The memory device of claim 29 further comprising pass transistors coupled to the plurality of sense amplifiers to select data from either the first bank of memory cores or the second bank of memory cores.

33. (Original) A memory device comprising:

a first bank of memory cores;

a second bank of memory cores, wherein the first bank of memory cores and the second bank of memory cores are interleaved in a first row on the memory device;

a plurality of sense amplifiers shared between the first bank of cores and the second bank of cores;

a column decoder; and

a plurality of column decode conductors coupled to the column decoder and the plurality of sense amplifiers, the plurality of column decode conductors being substantially parallel to the first row on the memory device.

34. (Original) The memory device of claim 33 further comprising:

a plurality of rows of which the first row is one; and

a plurality of columns of memory cores, each of the plurality of columns of memory cores having non-interleaved memory cores from a plurality of banks.

35. (Original) The memory device of claim 33 further comprising:

a third bank of memory cores;

a fourth bank of memory cores; and

a plurality of sense amplifiers shared between the third bank of memory cores and the fourth bank of memory cores;

wherein the third bank of memory cores and the fourth bank of memory cores are interleaved in a second row parallel to the first row.

36. (Original) A memory device comprising:

a plurality of memory cores physically arranged in rows and columns and logically arranged into banks that share sense amplifiers, wherein memory cores arranged in a first row alternate between a first bank and a second bank.

37. (Original) The memory device of claim 36 further comprising:

a column decoder;

column decode conductors coupled between the column decoder and the sense amplifiers shared between the first bank and the second bank; and

sense nodes coupled to the sense amplifiers, arranged substantially parallel to the column decode conductors.

38. (Original) The memory device of claim 36 wherein memory cores in a second row are arranged to alternate between a third bank and a fourth bank.

39. (Original) The integrated circuit of claim 36 wherein each of the of columns includes non-interleaved memory cores from different banks.

40. (Original) A memory device comprising:

a plurality of memory cores physically arranged in rows and columns and logically arranged into banks that share sense amplifiers, wherein memory cores arranged in a first row alternate between a first bank and a second bank; and

column decode conductors arranged in the first row to cross memory cores from the first bank and the second bank.

41. (Original) The memory device of claim 40 further comprising:

a second row having interleaved memory cores from a third bank and a fourth bank; and

a second plurality of sense amplifiers shared between the third bank and the fourth bank.

42. (Original) The memory device of claim 40 wherein each of the columns includes non-interleaved memory cores from different banks.

43. (Original) A memory device comprising:

a plurality of memory cores physically arranged in a plurality of rows and a plurality of columns and logically arranged into banks;

wherein memory cores arranged in each of the plurality of rows alternate between two banks, and memory cores arranged in each of the plurality of columns are from a different bank.

44. (Original) The memory device of claim 43 further comprising sense amplifiers shared between memory cores in each of the plurality of rows.

45. (Original) The memory device of claim 44 further comprising column decode conductors dedicated to each row, each column decoder conductor passing over memory cores of two banks and no more.

46. (Original) A computer system comprising:

a processor; and

a memory device coupled to the processor, the memory device including:

a plurality of rows and columns of memory cores; and

a plurality of sense amplifiers positioned between memory cores within each row, wherein every other memory core within each row is assigned to a bank.

47. (Original) The computer system of claim 46 wherein each sense amplifier is shared between two banks.

48. (Original) The computer system of claim 46 further comprising a memory controller coupled to the processor and the memory device.

49. (Original) A computer system comprising:

a processor; and

a memory device coupled to the processor, the memory device including:

a first bank of memory cores arranged in a first row;

a second bank of memory cores interleaved with the first bank of memory cores in the first row;

a third bank of memory cores arranged in a second row; and

a fourth bank of memory cores interleaved with the third bank of memory cores in the second row.

50. (Original) The computer system of claim 49 wherein the memory device further includes:

a first plurality of sense amplifiers shared between the first bank of memory cores and the second bank of memory cores; and

a second plurality of sense amplifiers shared between the third bank of memory cores and the fourth bank of memory cores.

51. (Original) The computer system of claim 49 further comprising a memory controller coupled to the processor and the memory device.

52. (Original) A computer system comprising:

a processor; and

a memory coupled to the processor, the memory including:

a plurality of sense amplifiers;

a first bank of memory cores, each coupled to at least one of the plurality of sense amplifiers; and

a second bank of memory cores, each coupled to at least one of the plurality of sense amplifiers;

wherein the first bank of memory cores and the second bank of memory cores are arranged in a strip with the plurality of sense amplifiers.

53. (Original) The computer system of claim 52 wherein the memory further includes:
column decode conductors coupled to the plurality of sense amplifiers and
a column decoder to drive the column decode conductors.

54. (Original) The computer system of claim 52 further comprising a memory controller coupled to the processor and the memory device.

55. (Original) A computer system comprising:
a processor;
a memory controller coupled to the processor; and
a memory device coupled to the memory controller, the memory device including:
a plurality of memory cores logically arranged into Rambus-compatible banks and physically arranged into rows and columns, wherein each column includes interleaved memory cores from two different Rambus-compatible banks.

56. (Original) The computer system of claim 55 wherein the memory device includes sense amplifiers shared between memory cores of Rambus-compatible banks in each row.

57. (Previously Added) A multibank memory device allowing simultaneous access of some of a plurality of memory banks while suffering reduced noise in sense amplifiers, comprising:
a plurality of memory banks, each memory bank including a plurality of memory cores arranged in strips of rows and columns;
a plurality of sense amplifiers shared among the memory cores of different ones of the plurality of memory banks;
a plurality of column decoders, each column decoder exclusively accessing a row of

memory cores from only two of the plurality of memory banks wherein the memory cores are separated from each other in the strip by shared sense amplifiers whereby the memory cores of the strip alternate between the two memory banks.

58. (Previously Added) A memory architecture having n banks of memory banks which allows simultaneous access of some of the memory banks, comprising a plurality of memory banks, each memory bank including a plurality of memory cores arranged in rows, each row having an associated column decoder connected to each memory core of the row and each core of the row associated with only one of two memory banks.

59. (Previously Added) A multibank memory architecture allowing simultaneous access of some of a plurality of memory banks while suffering reduced noise in sense amplifiers, comprising:

a plurality of memory banks, each memory bank containing a plurality of memory cores arranged in strips, each strip containing two memory banks and the strip having cores arranged to be alternating between the two memory banks with sense amplifiers shared between the cores of the two memory banks.

60. (Previously Added) A multibank memory architecture allowing simultaneous access of some of a plurality of memory banks comprising a row of memory cores interspersed between shared sense amplifiers, each memory core being a part of one of N memory banks, the strip having the memory cores laid out so that no two memory cores of the same memory bank share a common sense amplifier.